copper.

68. (New) The method of claim 67 wherein the layer thickness of the layer of said soft metal consisting of grains having a size of not more than 50 nm is not less than 600 nm.

69. (New) The method of claim 21 wherein the layer thickness of the layer of said soft metal consisting of grains having a size of not more than 50 nm is not less than 600 nm.

REMARKS

Claims 21-24, 26-39, 41-59, 61, 62 and 67 are now in the application. Claim 21 has been amended to recite "grain sizes not less than 200 nm" in place of the term "sufficiently large so that a substantially scratch-free surface upon polishing in a subsequently conducted chemical mechanical polishing step is obtained" to address the Examiner's rejection of claim 21 under 35 USC § 112 concerning vagueness. In addition, claim 21 has been amended to include recitations from prior claim 25 and to further recite that the "grain size is not more than 50 nm" of the other layer that is deposited consistent with the last line of page 6 of the specification. Claim 24 has been amended to recite "has" in place of "having" as suggested by the Examiner and to address the objection to this claim.

Claim 39 has been amended to include recitations from prior claim 40 directed to the material of the first and second metal layers. Claim 50 has been amended as suggested by the Examiner to recite "comprises" in place of "comprising" and thereby addressing the rejection to this claim. Claim 52 has been amended to correct the spelling of "least" thereby addressing the objection to this claim. In addition, claim 52 has been amended to include recitations from prior claim 59 reciting depositing a hard dielectric layer between the amorphous barrier layer and conductive metal.

Claims 53, 54, 55, 56, 57, 58, 59 and 60 have been amended to recite "surrounded at least on three sides by" in place of "encapsulated in" for purposes of clarification and thereby addressing the objection to these claims. The objection to the drawings has been noted but is not deemed tenable since the use of reference figures "12" and "14" is for the purpose to identify

two separate oxide layers consistent with the disclosure at page 13, lines 9-13 of the specification. Accordingly, it is believed that corrected drawings are not deemed necessary.

The objections to the claims and rejection of claims 21-27 under 35 USC § 112, second paragraph have been overcome by the above amendments to the claims.

The rejections of claims 21-24, 27 and 63-65 under 35 USC § 102(d) as being anticipated by U.S. Patent 5,534,463 to Lee, *et al.* and of claims 21-23, 27 and 63-65 under USC § 102(e) as being anticipated by U.S. Patent 5,373,192 to Eguchi have been rendered moot by the amendment to claim 21 that includes recitations from prior claim 25, which was not rejected over these grounds.

The rejections of claims 21, 22 and 24-27 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 18-23 of U.S. Patent 6,030,895 and of claims 28-38 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 7-17 of U.S. Patent 6,030,895 will be overcome by the filing of a Terminal Disclaimer upon an indication that the application is otherwise in condition for allowance. The filing of the Terminal Disclaimer is not to be construed as an admission, estoppel or acquiescence. See *Quad Environmental Technology v. Union Sanitary District*, 20 USPQ2d 1392 (Fed. Cir. 1991) and *Ortho Pharmaceuticals Corp. v. Smith*, 22 USPQ2d 1119 (Fed. Cir. 1992).

The rejection of claims 21-27 and 63-65 under 35 USC §102(e) as being anticipated by U.S. Patent 5,523,259 to Merchant, *et al.* has been overcome by the amendment to claim 21 and the cancellation of claims 63-65. In particular, claim 21 now recites "depositing a layer of said soft metal consisting of grains having a grain size of not more than 50 nm and a layer thickness of not less than 400 nm." In particular, Merchant fails to suggest employing a layer of a soft metal wherein the grain size is not more than 50 nm. Also, Merchant does not relate to improving the wear resistance as is the present invention, but instead relates to step filling of high aspect openings or vias. This according to Merchant is achieved by particular aluminum based layers having certain grain sizes and particular texture or grain orientation. Accordingly, since Merchant does not disclose a layer of 50 nm or less, Merchant does not anticipate these claims.

Claims 39-48 were rejected under 35 USC § 102(b) as being anticipated by U.S. Patent 5,262,354 to Cote, *et al.* Cote, *et al.* fail to anticipate claims 39 and 41-48. In particular, claim 39 has been amended to recite that the "first and second metal layer are deposited of a material selected from the group consisting of Al, Cu, Ag, CuAl, CuAg, AgAl and AuAgAl." These materials are considered to be soft metal conductors. On the other hand, the specific material for the metal layer 18 in Cote, *et al.* relied upon by the Examiner is a refractory metal such as titanium, tungsten, tantalum and various alloys thereof (*see* col. 7, lines 13-18 thereof). Accordingly, Cote, *et al.* does not anticipate claims 39 and 41-48.

Claims 52-62 were rejected under 35 USC § 102(d) as being anticipated by U.S. Patent 6,090,701 to Hasunuma, *et al.* Hasunuma, *et al.* failed to anticipate the above claims. In particular, claim 52 has been amended to include recitations from prior claim 60 that state "depositing a hard dielectric layer between said amorphous barrier layer and said conductive metal. On the other hand, Hasunuma, *et al.* failed to suggest providing such a layer. The layer 50 in Hasunuma, *et al.* is a niobium film (*See* col. 48, line 53 of Hasunuma, *et al.*). Accordingly, Hasunuma, *et al.* fail to anticipate claims 52-59, 61 and 62.

The rejection of claims 49-51 under 35 USC § 103(a) as being unpatentable over Merchant, *et al.* in view of U.S. Patent 5,709,958 to Toyoda, *et al.* is not deemed tenable. In particular as discussed above, Merchant, *et al.* relates to filling high aspect openings or via with an aluminum-base plug. Crucial to the suggestions in Merchant, *et al.* is the use of three sub-layers of aluminum of particular grain size as well as the particular texture or grain orientation to substitute copper for the aluminum required by Merchant would be contrary to the suggestions in Merchant. Furthermore, Toyoda, *et al.* fail to discuss any particular grain size or grain orientation for the various metals alluded to therein. Accordingly, the prior art lacks the motivation to employ copper which would contrary to the objectives and suggestions in Merchant, *et al.*

With respect to novelty, the cited references fail to anticipate the present invention. In particular, anticipation requires the disclosure, in a prior art reference, of each and every recitation as set forth in the claims. *See Titanium Metals Corp. v. Banner*, 227 USPQ 773 (Fed. Cir. 1985), *Orthokinetics, Inc. v. Safety Travel Chairs, Inc.*, 1 USPQ2d 1081 (Fed. Cir. 1986), and *Akzo N.V. v. U.S. International Trade Commissioner*, 1 USPQ2d 1241 (Fed. Cir. 1986).

There must be no difference between the claimed invention and reference disclosure for an anticipation rejection under 35 USC 102. *See Scripps Clinic and Research Foundation v. Genetech, Inc.*, 18 USPQ2d 1001 (CAFC 1991) and *Studiengesellschaft Kohle GmbH v. Dart Industries*, 220 USPQ 841 (CAFC 1984).

Concerning obviousness, the mere fact that cited art may be modified in the manner suggested by the Examiner does not make this modification obvious, unless the cited art suggest the desirability of the modification. No such suggestion appears in the cited art in this matter. The Examiner's attention is kindly directed to *In re Lee* 61 USPQ2d 1430 (Fed. Cir. 2002) *In re Dembiczak et al.* 50 USPQ2d. 1614 (Fed. Cir. 1999), *In re Gordon*, 221 USPQ 1125 (Fed. Cir. 1984), *In re Laskowski*, 10 USPQ2d. 1397 (Fed. Cir. 1989) and *In re Fritch*, 23, USPQ2d. 1780 (Fed. Cir. 1992).

In Dembiczak et al., supra, the Court at 1617 stated: "Our case law makes clear that the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references. *See, e.g., C.R. Bard, Inc., v. M3 Sys., Inc.*, 157 F.3d 1340, 1352, 48 USPQ2d. 1225, 1232 (Fed. Cir. 1998) (describing 'teaching or suggestion motivation [to combine]' as in 'essential evidentiary component of an obviousness holding'), *In re Rouffet,* 149 F.3d 1350, 1359, 47 USPQ2d. 1453, 1459 (Fed. Cir. 1998) ('the Board must identify specifically...the reasons one of ordinary skill in the art would have been motivated to select the references and combine them');...".

Also, the cited art lacks the necessary direction of incentive to those of ordinary skill in the art to render the rejection under 35 USC 103 sustainable. The cited art fails to provide the degree of predictability of success of achieving the properties attainable by the present invention needed to sustain a rejection under 35 USC 103. *See Diversitech Corp. v. Century Steps, Inc.* 7 USPQ2d 1315 (Fed. Cir. 1988), *In re Mercier*, 185 USPQ 6 (CCPA 1977), *In re Estes*, 164 USPQ (CCPA 1970), and *In re Papesch*, 137 USPQ 43 (CCPA 1963).

Moreover, the properties of the subject matter and improvements which are inherent in the claimed subject matter and disclosed in the specification are to be considered when evaluating the question of obviousness under 35 USC 103. *See Gillette Co. v. S.C. Johnson &*

Son, Inc., 16 USPQ2d. 1923 (Fed. Cir. 1990), *In re Antonie*, 195, USPQ 774 (CCPA 1975) and *In re Naylor*, 152 USPQ 106 (CCPA 1966).

No property can be ignored in determining patentability and comparing the claimed invention to the cited art. Along these lines, *see In re Papesch*, supra, *In re Burt, et al.* 148 USPQ 548 (CCPA 1966), *In re Ward*, 141 USPQ 227 (CCPA 1964), and *In re Cescon*, 177 USPQ 264 (CCPA 1973).

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

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APPENDIX
Claims With Markings to Show Changes Made

21. (Amended) A method of making a soft metal conductor for use in a semiconductor device [comprising the step of] which comprises depositing a first layer of said soft metal consisting of grains having grain sizes [sufficiently large such that a substantially scratch-free surface upon polishing in a subsequently conducted chemical mechanical polishing step is obtained] not less than 200 nm; and further comprising depositing a layer of said soft metal consisting of grains having a grain size of not more than 50 nm and a layer thickness of not less than 400 nm prior to said deposition process of said first layer of soft metal so as to provide a substantially scratch-free surface upon polishing in a subsequent CMP step.

24. (Amended) A method according to claim 21, wherein said first soft metal layer [having] has a thickness of at least 100 nm.

39. (Amended) A dual-step deposition method for making a soft metal conductor for use in an electronic device comprising [the steps of]:

depositing a first layer of metal by a physical vapor deposition process to a first thickness, and

depositing a second layer of metal on top of said first layer of metal to a second thickness larger than said first thickness by a method selected from the group consisting of chemical vapor deposition, electroplating and electroless plating; and

wherein said first and said second metal layer are deposited of a material selected from the group consisting of Al, Cu, Ag, CuAl, CuAg, AgAl and CuAgAl.

50. (Amended) A method for forming an interconnect in a logic of memory device according to claim 49, wherein said at least one layer of metal [comprising] comprises two layers of metal deposited into a line or via hole.

52. (Amended) A method for forming an interconnect surrounded at least on three sides by an amorphous barrier layer comprising [the steps of]

depositing an amorphous barrier layer of refractory metal nitride or carbide into a line or via a hole by a vapor deposition technique, and

depositing a layer of a conductive metal having an average grain size of not smaller than 0.3μm on top of said amorphous barrier layer filling said line or via hole; and

further comprising depositing a hard dielectric layer between said amorphous barrier layer and said conductive metal.

53. (Amended) A method for forming an interconnect [encapsulated in] surrounded on three sides by an amorphous barrier layer according to claim 52, wherein said refractory metal in said refractory metal nitride or carbide is selected from the group consisting of W, Ta and Ti.

54. (Amended) A method for forming an interconnect [encapsulated in] surrounded at least on three sides by an amorphous barrier layer according to claim 52, wherein said conductive metal is selected from the group consisting of Cu, Ag, Al, CuAg, CuAl, AgAl and CuAgAl.

55. (Amended) A method for forming an interconnect [encapsulated in] surrounded at least on three sides by an amorphous barrier layer according to claim 52, wherein said vapor deposition technique is a chemical vapor deposition technique.

56. (Amended) A method for forming an interconnect [encapsulated in] surrounded at least on three sides by an amorphous barrier layer according to claim 52, wherein said refractory metal nitride is deposited by a chemical vapor deposition technique conducted at a reaction temperature about 300°C and about 400°C.

57. (Amended) A method for forming an interconnect surrounded [in] at least on three sides by an amorphous barrier layer according to claim 52, wherein said refractory metal nitride is deposited by a sputtering technique by using a composite target.

58. (Amended) A method for forming an interconnect [encapsulated] surrounded [in] at least on three sides by an amorphous barrier layer according to claim 52 further

comprising the step of annealing said amorphous barrier layer at a temperature of not lower than 400°C for at least ½ hour prior to the conductive metal deposition step.

59. (Amended) A method for forming an interconnect [encapsulated in] surrounded at least on three sides by an amorphous barrier layer according to claim 52 further comprising the step of depositing a seed layer of said conductive layer prior to the conductive metal deposition step.

62. (Amended) A method for forming [a large grain] an interconnect [encapsulated in] surrounded at least on three sides by an amorphous barrier layer according to claim [59] 52, wherein said hard dielectric layer is deposited of a material selected from the group consisting of fluorinated oxide and amorphous or porous oxide treated with SiH_4 or CH_4.